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AMS02 - PDS

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1. SCOPE

The document corresponds to contract deliverable DEL098.
The aim of this document is to provide a brief description of the AMS02 – PDS (Power Distribution System) TMM and GMM, and to present the results of the performed thermal analysis.

2. ACRONYM LIST

A

ABCL	As-Built Configuration data List
ADP	Acceptance Data Package
AR	Acceptance Review
ATP	Authorization To Proceed

B

BC	Back Cover
BP	Back Panel

C

CAD	Computer Aided Design
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CI	Configuration Item
CIDL	Configuration Item data List

D

DRD	Document Requirements Description

E

EGSE	Electrical Ground Support Equipment
EM	Engineering Model

F

FEM	Finite Element Model
FFMAR	Final Flight Model Acceptance Review
FM	Flight Model

G

GSE	Ground Support Equipment
GMM	Geometrical Mathematical Model

H

HW	Hardware

I

ICD	Interface Control Document
I/F	Interface
ISS	International Space Station

J

JSC	Johnson Space Center

K

KSC	Kennedy Space Center

L

M

N

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NA Not Applicable
NASA National Aeronautics and Space Administration
NCR Non Conformance Report
NRB Non-conformance Review Board
NSTS National Space Transportation System (Shuttle)

O

P
PA Product Assurance
PB2 Power Board 2
PCB Printed Circuit Board
PDR Preliminary Design Review
PDS Power Distribution System

Q
QM Qualification Model

R
RFD Request For Deviation
RFW Request For Waiver

S
STS Space Transportation System (Shuttle)
SW Software

T
TBC To Be Confirmed
TBD To Be Defined
TRB Test Review Board
TRR Test Readiness Review
TMM Thermal Mathematical Model

3. RELEVANT DOCUMENTS

Documents here below identified are applicable and/or reference for the activities described in the present document and are considered part of it to the extent specified herein.

3.1 APPLICABLE DOCUMENTS

AD #	Doc Number	Issue	Date	Rev	Title
1	**AMS-RQ-CGS-002**	1	April 2007		POWER DISTRIBUTION SYSTEM (PDS) SPECIFICATIONS
2	**AMSCD-PL-CGS-001**	1	04/02/2008		AMS02 PA Plan
3	**DC-IPC-2007-062**	1	09/05/2007	A	CAPITOLATO TECNICO AMS-02

3.2 REFERENCE DOCUMENTS

RD #	Doc Number	Issue	Date	Rev	Title

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4. SYSTEM DESCRIPTION

The PDS is the Power Distribution System for the AMS-02 payload and it is the power interface of the AMS-02 System to ISS.
The PDS unit is composed of two identical parts in cold redundant configuration. Each of the two sections includes the following electronic boards:

- N.1 ESEM1-A board
- N. 4 PB2 boards
- N. 4 ESEM3-A boards
- N. 1 ESEM3-B board
- N.1 CAN bus I/F board (USCM)

Additionally, each section are provided with 1 input stage board (with EMI filter and current telemetry)

The two sections are enclosed in a mechanical box which provides the unit housing and which is also the main thermal interface to radiator.

4.1 TCS CONCEPTS

PDS Thermal Control is achieved by proper passive dissipation of on-board produced heat in hot environmental conditions, while it shall provide thermal heating to keep the minimum operative temperature in cold environments.

The PSD heat dissipation shall be based on AMS-02 WAKE radiator, where the PDS is flat-mounted.

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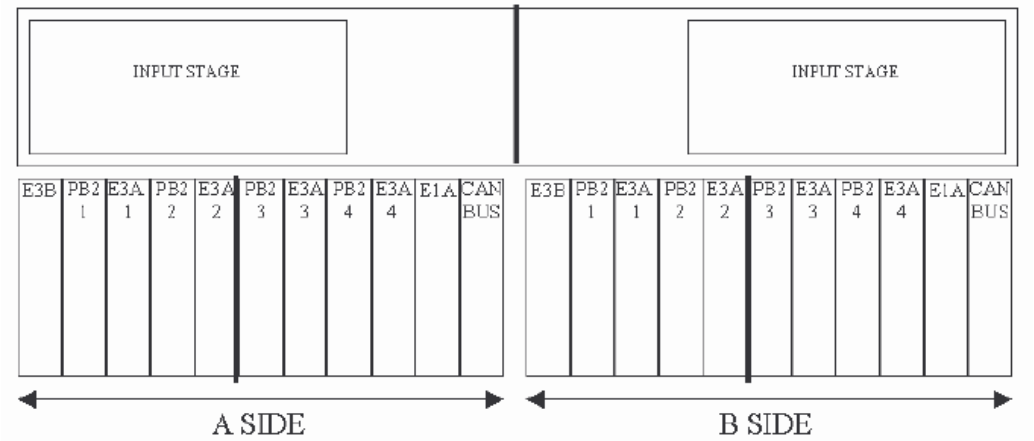
5. MODEL DESCRIPTION

5.1 SUBMODELS

The PDS TMM and GMM have been divided in different sub-models. Each sub-model represents a different elements The table below show all the sub-models name with their description.

BOX	PDS Box
PB22A	PB2#2 bus A
PB23A	PB2#3 bus A
PB24A	PB2#4 bus A
ESEM3BA	ESEM3B bus A
ESEM3A1A	ESEM3A#1 bus A
ESEM3A2A	ESEM3A#2 bus A
ESEM3A3A	ESEM3A#3 bus A
ESEM3A4A	ESEM3A#4 bus A
ESEM1AA	ESEM1A bus A
CANBA	CAN bus A
PB21B	PB2#1 bus B
PB22B	PB2#2 bus B
PB23B	PB2#3 bus B
PB24B	PB2#4 bus B
ESEM3BB	ESEM3B bus B
ESEM3A1B	ESEM3A#1 bus B
ESEM3A2B	ESEM3A#2 bus B
ESEM3A3B	ESEM3A#3 bus B
ESEM3A4B	ESEM3A#4 bus B
ESEM1AB	ESEM1A bus B
CANBB	CAN BUS B
INPUTSA	INPUT STAGE bus A
INPUTSB	INPUT STAGE bus B
PWB2_N1A	PB2#1 bus A – detailed model

The figure below show the position of each board in the PDS box. A side and B side are symmetric.



Since PB2 is a critical item, one PB2 board has been more detailed analyzed. PWP2_N1A is the detailed submodel of PB2 board.

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5.2 OPTICAL PROPERTIES USED

The following table summarized the optical properties used in GMM to calculate radiative links. In order to consider an hot worst case, only EOL properties has been considered.
Since no flux in visible spectrum has been considered, α has been assumed to be 1 for all materials.

Tab 5-1 - used optical properties

	ε
Black paint (midwall – sidewall internal)	0.84
Alodine (Box)	0.25
Board (PCB)	0.70
Mosfet	0.50
NA (inductors – transformers, etc)	0.85

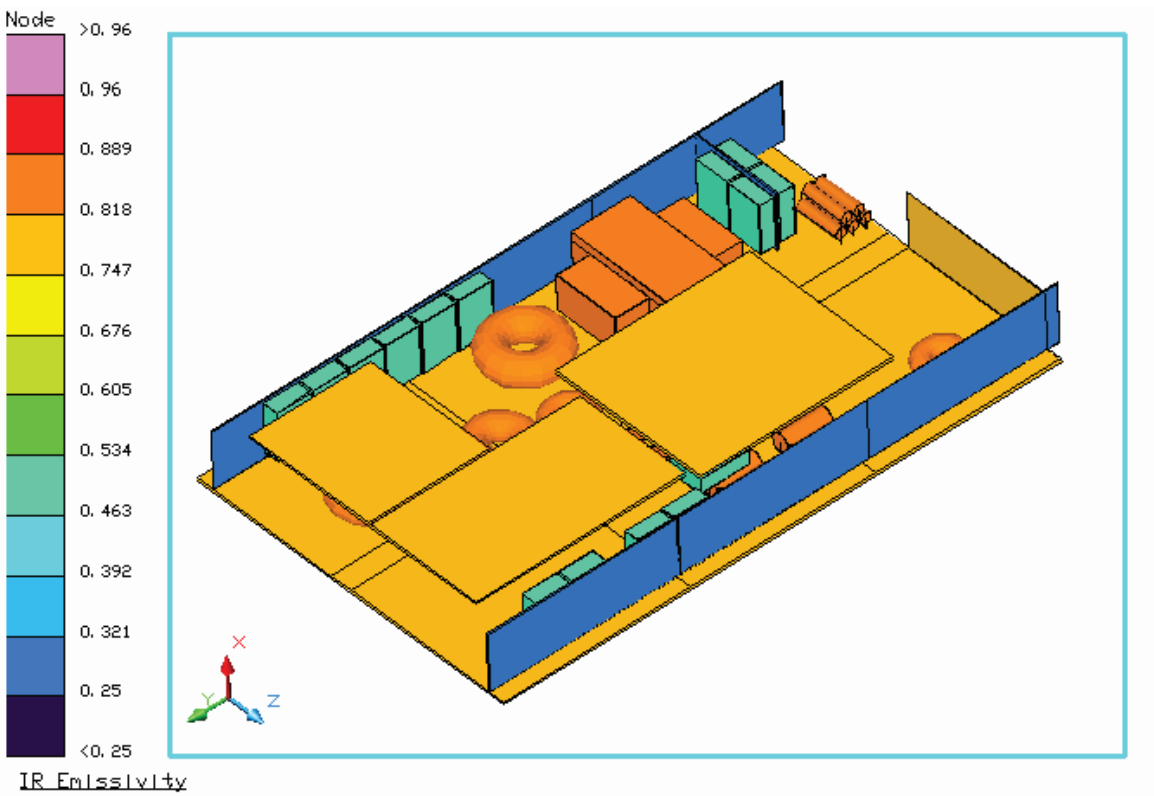

Fig 5-1 - Optical properties used - detailed PB2 board

5.3 ELECTRICAL BOARD CONNECTION INTERFACE

All the electrical board have a similar interface layout to the base plate. The sketch below shows this layout.

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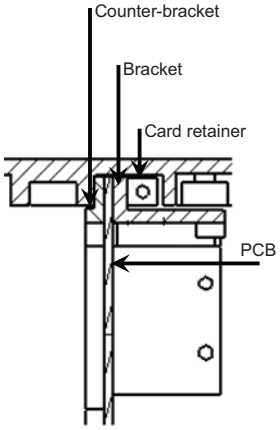

This is a critical interface, since the whole heat flux pass from the board to base plate (and so to radiator) through this interface. For this reason a detailed nodal breakdown for this zone has been used.
For ESEM1A, ESEM3A and ESEM3B the following network has been used:

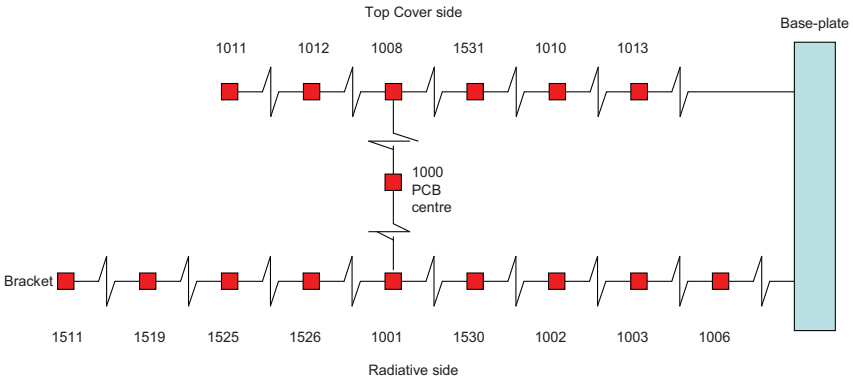

Fig 5-2 - Interface PCB to base-plate network

Tab 5-2 - Conductor in PCB interface

From node	***To node***	***Description***
1013	1010	Material conductance to base-plate node
1010	1531	Contact conductance by card retainer
1531	1008	Conductance by screws – counter-bracket PCB
1008	1012	Contact conductance from PCB to bracket
1011	1012	Bracket
1006	1003	Material conductance to base-plate node
1003	1002	Contact conductance by card retainer
1002	1530	Conductance by screws – counter-bracket PCB
1530	1001	Internal PCB conductance
1001	1526	Internal PCB conductance
1526	1525	Conductance by screws –bracket PCB
1525	1519	Bracket internal conductance
1519	1511	Bracket internal conductance

Further details for each board will be given in dedicated chapter.

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5.4 BOX

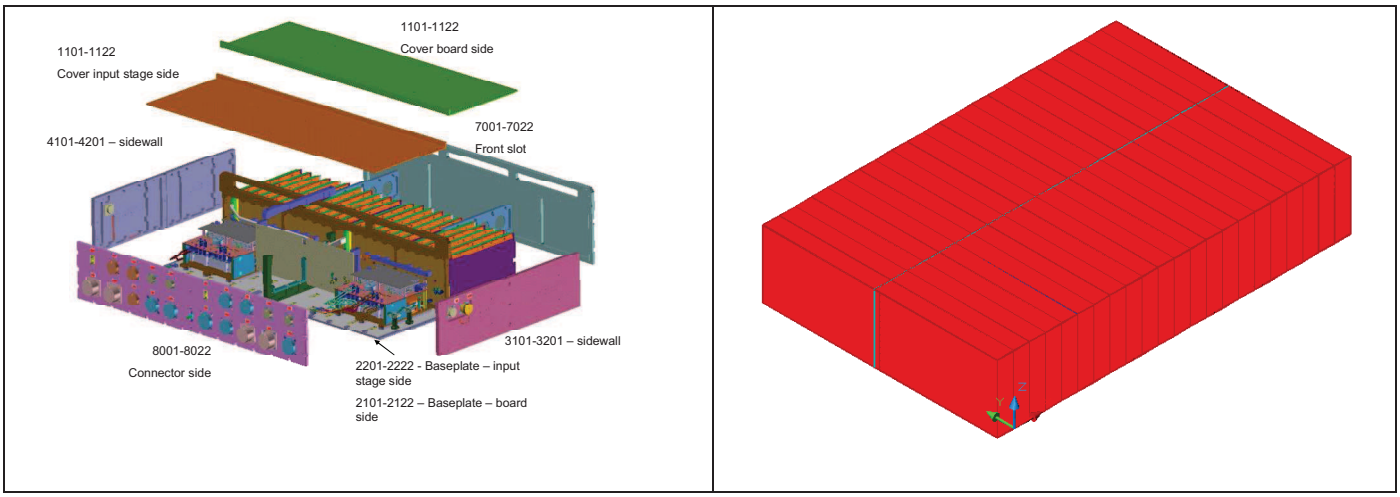

Fig 5-3 - PDS box

For the box the following nodal breakdown has been used (128 nodes total):

- 44 nodes for base plate
- 44 nodes for top cover
- 22 nodes for front wall
- 22 nodes for connector side
- 2 nodes for each side wall
- 2 nodes for internal frames

PDS box is made of aluminum: for material thermal properties the following values have been used:

Conductivity	155 W/Km
Thermal capacitance	800 J/kgK
Density	2700 kg/m3

5.5 PDS POWER DISSIPATION CASE

In order to analyze the worst hot case, the PDS power dissipation corresponding to the step 4.0 @ 112V on PDS power budget has been used. The following table summarized the dissipation for each board in this configuration.

Tab 5-3 - PDS power distribution

PWB2_N1A	62.32 W	PB21B	0.00 W
PB22A	56.23 W	PB22B	0.00 W
PB23A	49.58 W	PB23B	0.00 W
PB24A	45.80 W	PB24B	0.00 W
ESEM3BA	6.74 W	ESEM3BB	0.00 W
ESEM3A1A	15.57 W	ESEM3A1B	0.00 W
ESEM3A2A	16.61 W	ESEM3A2B	0.00 W
ESEM3A3A	15.19 W	ESEM3A3B	0.00 W
ESEM3A4A	14.55 W	ESEM3A4B	0.00 W
ESEM1AA	24.67 W	ESEM1AB	0.00 W
CANBA	6.24 W	CANBB	6.24 W
INPUTSA	43.06 W	INPUTSB	0.00 W
Total			***363 W***

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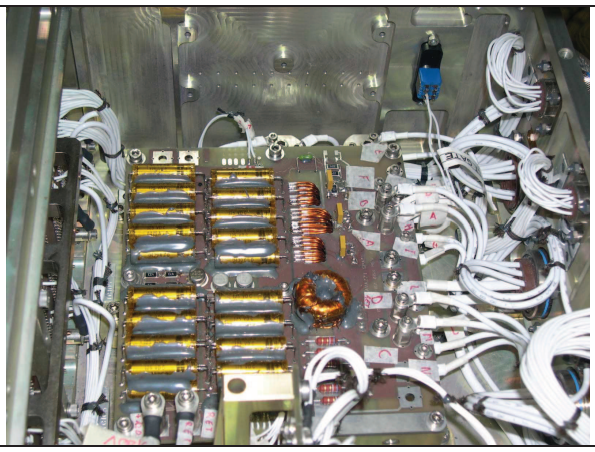
5.6 INPUT STAGES

Input stages A and input stage B have been identically nodalized. A total of 12 nodes for each input stage have been used, as follows:

- 4 nodes for structure
- 5 nodes for mosfets
- 2 nodes for inductances
- 1 node for PCB



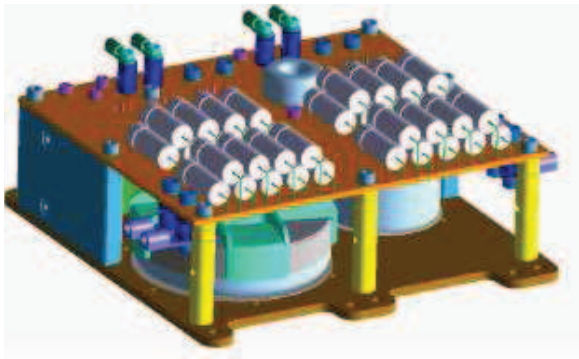


Fig 5-4 - Input stage

The following table show the power applied to the model in order to simulate internal dissipations:

PCB	6.24W
Mosfet	2.95W each
Inductances	10.02W each

5.7 CAN BUS

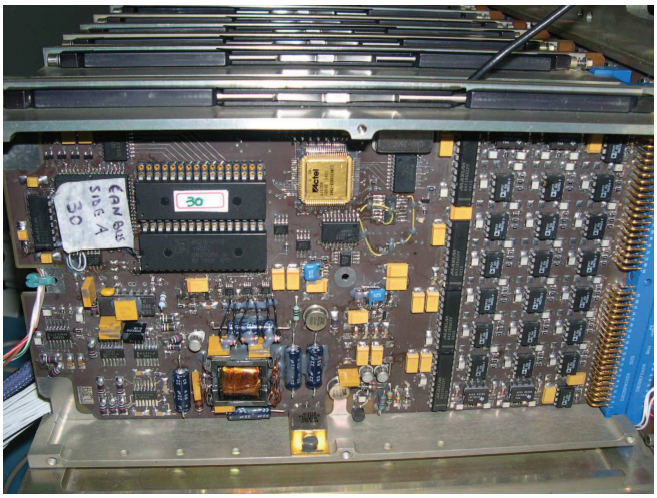


Fig 5-5 - Can bus

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For CAN bus boards, the following nodal breakdown has been used:

- 1 node for PCB
- 15 nodes for PCB interaction to base plate (bracket/counter-bracket/card retainer)
- 1 node for top cover

All the dissipated power is applied on PCB node.

5.8 ESEM3B

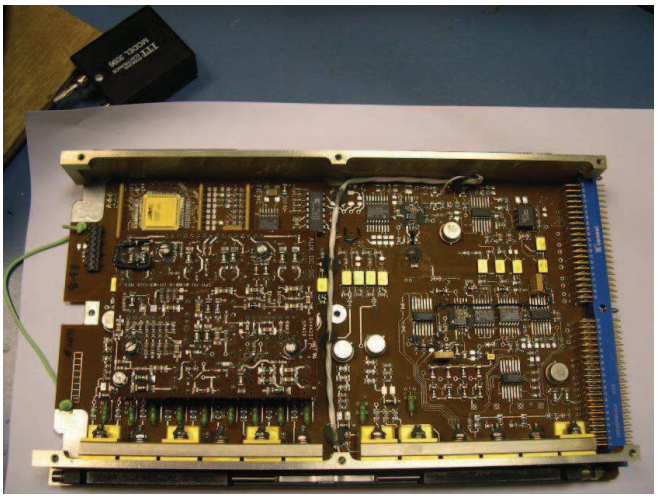

Fig 5-6 - Esem3b

The ESEM3B board is composed by a PCB on which 18 mosfet are installed. The following nodal breakdown has been used:

- 1 node for PCB
- 15 nodes for PCB interaction to base plate (bracket/counter-bracket/card retainer)
- 1 node for top cover
- 18 nodes for mosfet
- 18 nodes for mosfet cases

The following table show the power applied to the model in order to simulate internal dissipations:

PCB	3.12W
Mosfet	0.2010W each

5.9 ESEM3A

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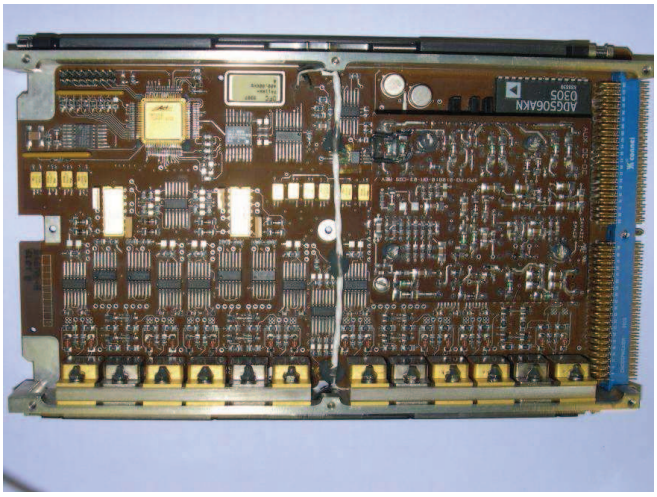

Fig 5-7 - Esem3a board

The ESEM3A board is composed by a PCB on which 24 mosfets, on two rows of 12 each, are installed. The following nodal breakdown has been used:

- 1 node for PCB
- 15 nodes for PCB interaction to base plate (bracket/counter-bracket/card retainer)
- 1 node for top cover
- 24 nodes for mosfet
- 24 nodes for mosfet cases

The following table show the power applied to the model in order to simulate internal dissipations:

	ESEM3A1	ESEM3A2	ESEM3A3	ESEM3A4
PCB	5.17W	5.17W	4.79W	4.15W
Mosfet	0.433W each	0.433W each	0.433W each	0.433W each

5.10 ESEM1A

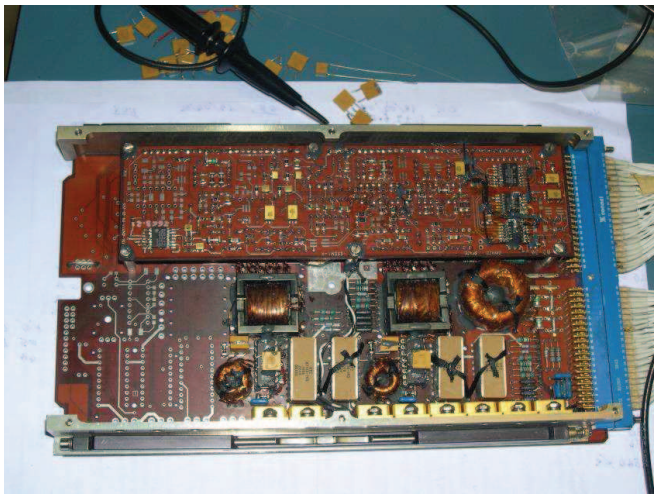

Fig 5-8 - Esem1a

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The ESEM1A board is composed by a PCB on which 8 mosfet are installed. The following nodal breakdown has been used:

- 1 node for PCB
- 15 nodes for PCB interaction to base plate (bracket/counter-bracket/card retainer)
- 1 node for top cover
- 8 nodes for mosfets

The following table show the power applied to the model in order to simulate internal dissipations:

PCB	3.70W
Mosfet	2.62W each

5.11 PB2

Due to its dissipation (more than 62W can be dissipated when supplied at 110V), PB2 boards are critical items in PDS thermal control system. For this reason a more detailed network has been used for analysis.
A detailed GMM has been also used to compute internal radiative links.

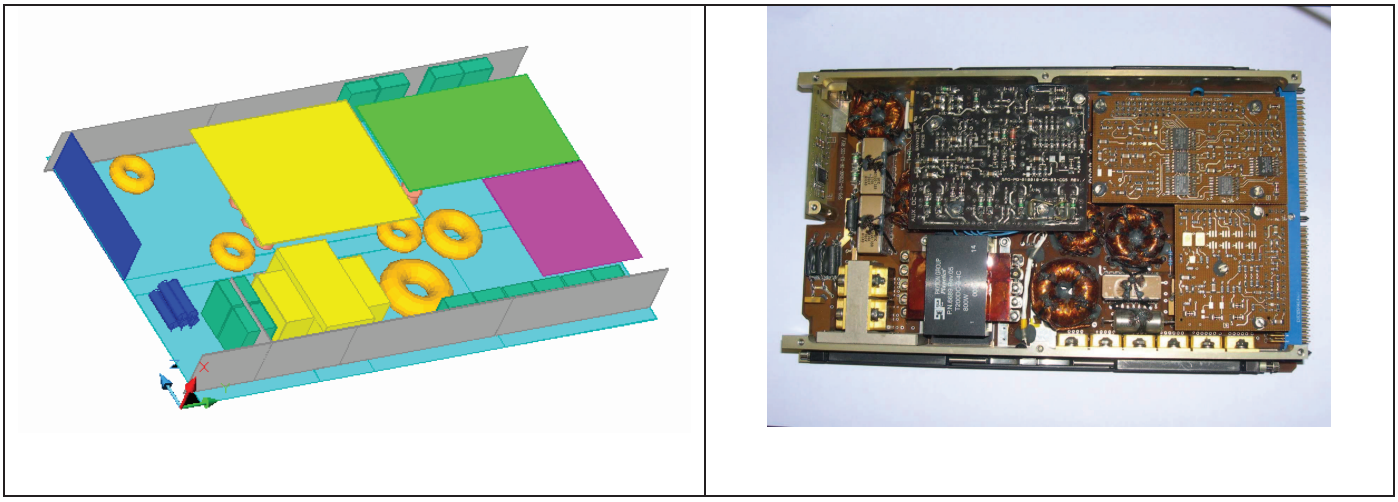

Fig 5-9 – PB2 GMM and PB2 layout

Detailed PB2 model contain (90 nodes total for each PB2):

- 7 nodes for main PCB
- 3 nodes for each bracket (6 total)
- 1 node for T bracket
- 1 node for each electrical item (snubbers, mosfet, inductors, etc – 34 nodes total see table for details)
- 1 node for transformer
- 1 node for transformer plate (connected to PCB)
- 1 node for each mezzanine PCB (3 in total)
- 18 nodes for board interface to base-plate radiative side
- 18 nodes for board interface to base-plate cover plate side

Tab 5-4 - PB2 components nodes

Node ID	Description	Node ID	Description
3100	Transformer T1	**3402**	Mosfet SECONDARY Q6
3101	Mosfet output Q21	**3403**	Mosfet SECONDARY Q7
3102	Mosfet output Q20	**3404**	Mosfet SECONDARY Q8

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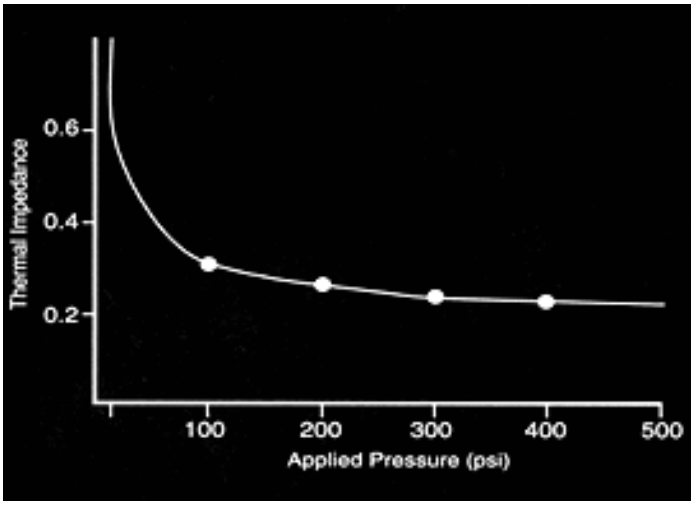
3103	Mosfet output Q25	**3500**	Mosfet on Mezzanine
3104	Mosfet output Q24	**3600**	controller
3110	L3 inductor	**3701**	Tantalium Condenser
3120	TD2 transformer	**3702**	Tantalium Condenser
3140	L4 inductor (L LEAKAGE)	**3800**	Snubber resistors
3150	L5 inductor (L DIFF)	**3901**	DRIVERS transistors
3160	L1 inductor (L COMMON)	**3902**	DRIVERS transistors
3201	Mosfet In-rush Q10	**3903**	DRIVERS transistors
3202	Mosfet In-rush Q11	**3904**	DRIVERS transistors
3301	Mosfet PRIMARY Q4	**3905**	DRIVERS transistors
3302	Mosfet PRIMARY Q1	**3906**	DRIVERS transistors
3303	Mosfet PRIMARY Q3	**3907**	DRIVERS transistors
3304	Mosfet PRIMARY Q2	**3908**	DRIVERS transistors
3401	Mosfet SECONDARY Q5	**3909**	DRIVERS transistors

For PB2 interface to base-plate a quite different network than other boards has been used. The necessity to modelling different interface lead to consider a network like the one shown in the picture below.
Critical interfaces (PCB to bracket and counter-bracket and counter-bracket to base-plate) have been studied to ensure a better heat flux towards the radiator. As result some filler material interface have been foreseen.
Cho-Therm 1671 with pressure sensitive adhesive has been foreseen for interface counter-bracket to base-plate, and Therm-a-form T642 shall instead be used between PBC and both counter-bracket and bracket.
These interfaces have been modelled with a conductance given by a contact conductance multiplied for the contact area.
The following contact conductance value have been used for Chotherm and .Therm-a-form. A wide margin has been taken in account considering materials datasheet values.

Tab 5-5 - Contact conductance used for Cho-Therm and therm-a-form T642

Interface materials	**Used contact conductance**	**Datasheet contact conductance**
Cho-Therm 1671	2000 W/K*m2	5000 W/K*m2
Therm-a-form T642 (0.1mm thick layer)	3500 W/K*m2	12000 W/K*m2

For Cho-Therm, datasheet value has been computed referring to the following graph, that shows the curve of thermal impedance vs applied pressure. The pressure of about 170 psi is provided by the card-retainer.



An impedance of 0.3 K*inc^2/W (1.94 K*cm^2/W) that correspond to a thermal contact conductivity of 5154W/m^{2}K.

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Therm-a-form thermal conductivity is shown in the vendor table below:

Property	T642
Binder	Silicone
Filler	Boron Nitride
Color	Blue
Mix Ratio, Part A:B (by weight or volume)	10:1
Pot Life, hours @ 20°C	1
Cure Cycles	3 minutes @ 150°C 30 minutes @ 70°C 48 hours @ 23°C
Solvent Extractables, %	1-2
Thermal Conductivity, W/m-K	1.2
Dielectric Strength, Vac/mil	500
Volume Resistivity, ohm-cm	1×10^{13}
Hardness (Shore A)	70
Viscosity, poise	2500
Outgassing[1] % TML % CVCM	 0.32 0.21
Specific Gravity	1.5
Shelf Life	3 months @ 20°C 6 months @ 0°C 12 months @ –40°C
Continuous Use Temperature	–50°C to +150°C

[1] Material cured 24 hours at 150°C

Consider a 0.1mm layer (conservative value) the conductance through the glue layer is 12000W/m^{2}K. since glue layer thickness is hard to control during integration, a wide margin on datasheet value has been taken in account.

The need and the importance of these interface material will be shown in chapter 6.4 .

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6. ANALYSIS RESULTS

According with AD1:

> ***4.3.1.2.6 COMPONENTS TEMPERATURE LIMITS***
> *The equipment component temperature shall not exceed the following appropriate maximum values:*
> - *life derated value when the equipment is at the maximum flight operating temperature;*
> - *rated value, when the equipment is at its maximum qualification temperature limits.*

and in order to simulate the worst case for PDS a steady state analysis has been performed. PDS box temperature (TRP Thermal Reference Point) has been maintained at the worst hot temperature foreseen in PDS life (48℃).
A further steady state analysis with the box temperature at 53℃ (5℃ higher than the worst temperatur e) has been performed. This shall be the base plate test temperature in the qualification thermal vacuum test.

Cold cases have not been analyzed since the correct sequence of heaters turning on (analyzed on wake radiator analysis) shall permit the correct working of PDS in cold cases.

Transient analysis have not been performed since not dimensioning.

6.1 PDS THERMAL REFERENCE POINT TEMPERATURE

The temperatures for PDS base-plate (TRP) are given as output from WAKE radiator analysis. The worst hot case for these analysis give the following temperature for PDS box nodes. Since heat pipe layout is not symmetric on radiator, different scenario are possible when bus A or bus B are working.

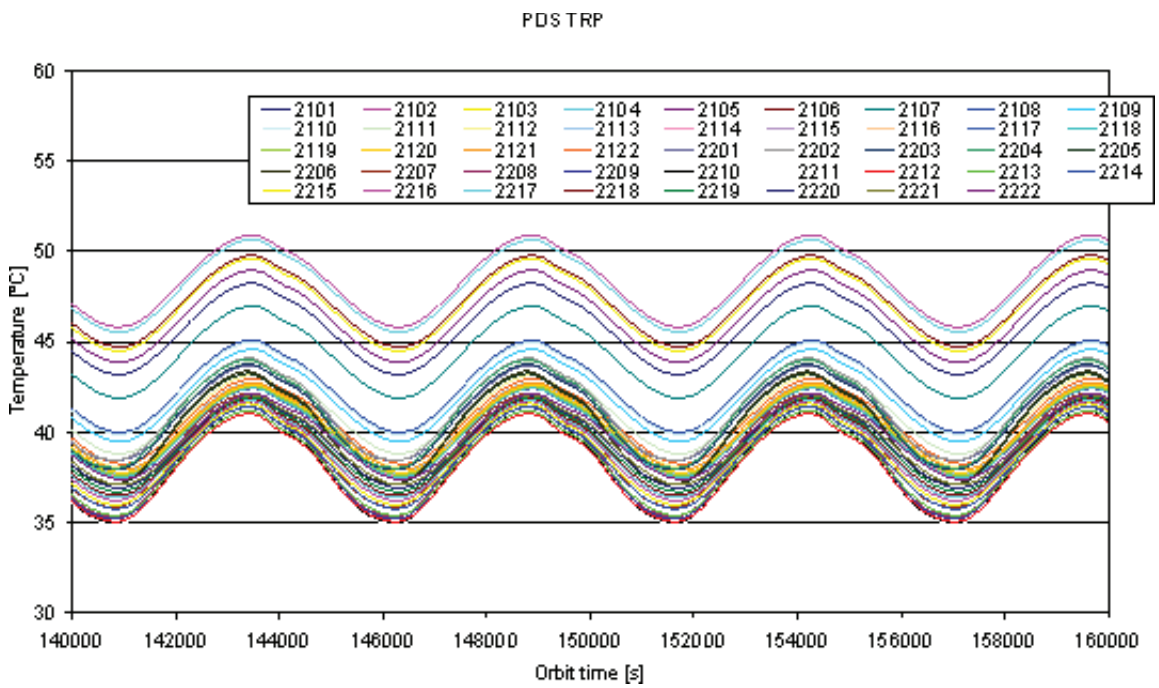

Fig 6-1 - PDS box temperature in worst hot case - Bus A on

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	Analysis details
Analysis ID	**1**
Optical Properties	**EOL**
I/F Data Rationale	I/F data have been generated considering AMS ON in the worst HOT.
I/F Data Files	IF_B-75-15_15-15_hot_v4_2_latest MLI_BusA
AMS Status	ON
PDS Heater power	OFF
Radiator Heater power	OFF
PDS power	365 W (bus A)
CRATES power	428 W
CAB power	105 W
Results	
Max temperature PDS	50.92℃ (2102)

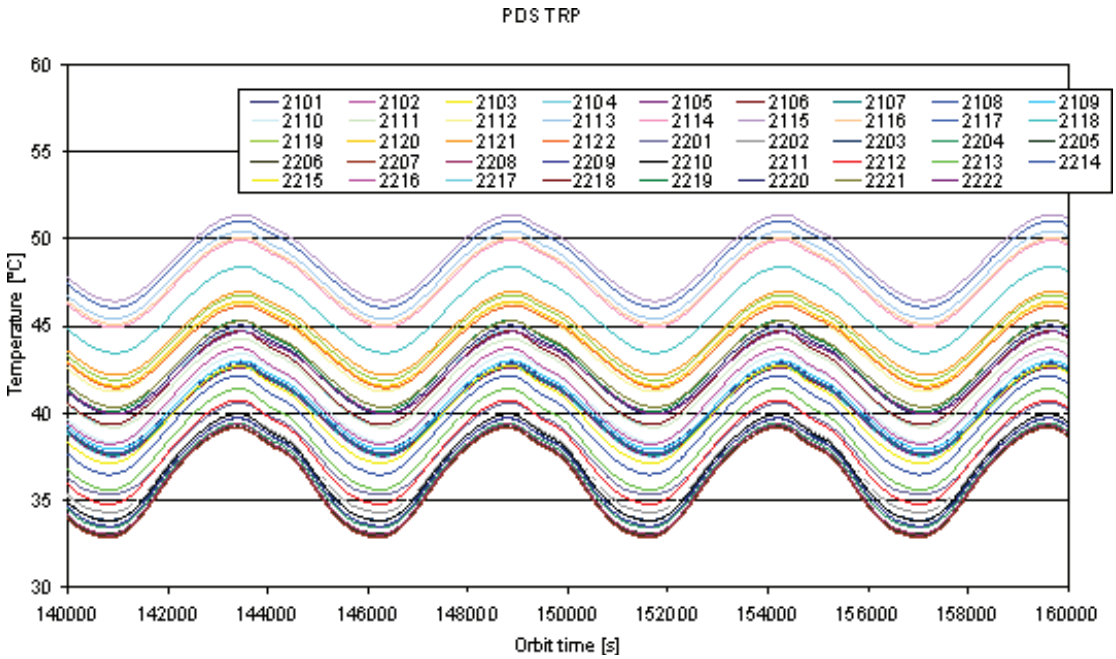

Fig 6-2 - PDS box temperature in worst hot case - Bus B on

	Analysis details
Analysis ID	**1**
Optical Properties	**EOL**
I/F Data Rationale	I/F data have been generated considering AMS ON in the worst HOT.
I/F Data Files	IF_B-75-15_15-15_hot_v4_2_latest MLI_BusB
AMS Status	ON
PDS Heater power	OFF
Radiator Heater power	OFF
PDS power	365 W (bus B)
CRATES power	428 W
CAB power	105 W
Results	
Max temperature PDS	51.4℃ (T.2115)

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Maximum PDS TRP temperature is 51.4℃, that is below test temperature. This "worst hot" configurations (combination of worst beta angle and worst ISS attitude) is not the nominal one.
More frequent ISS attitude is know as MPA (Minimum Propellant Attitude); in this configuration maximum PDS TRP temperature are lower, as shown in the graphs below:

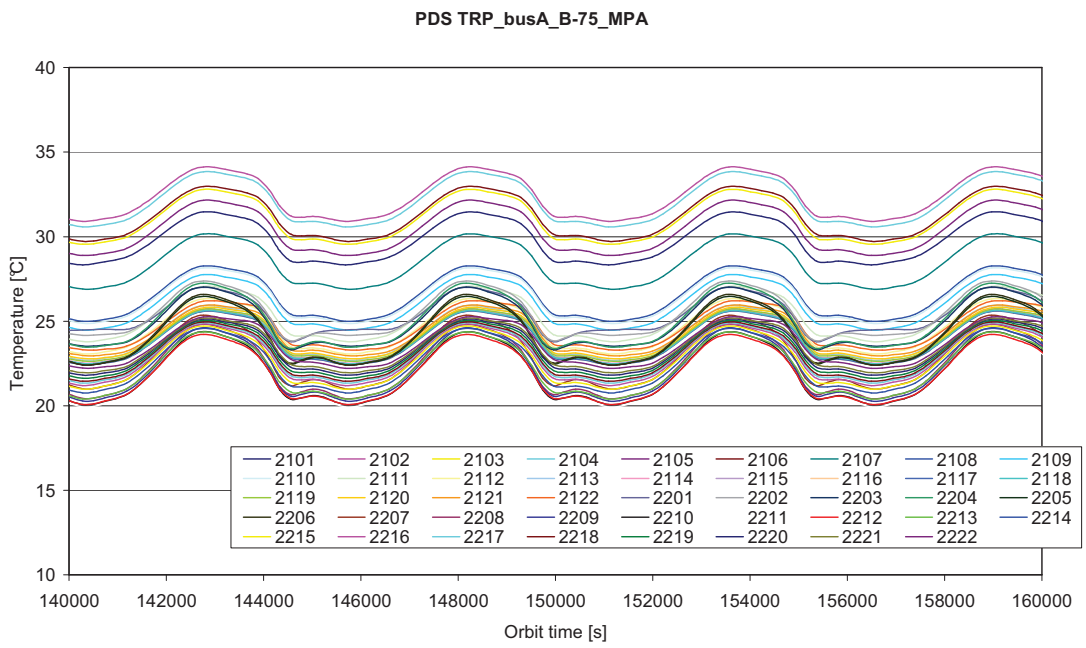

Fig 6-3 - PDS box temperature in worst hot orbit at nominal attitude - Bus A on

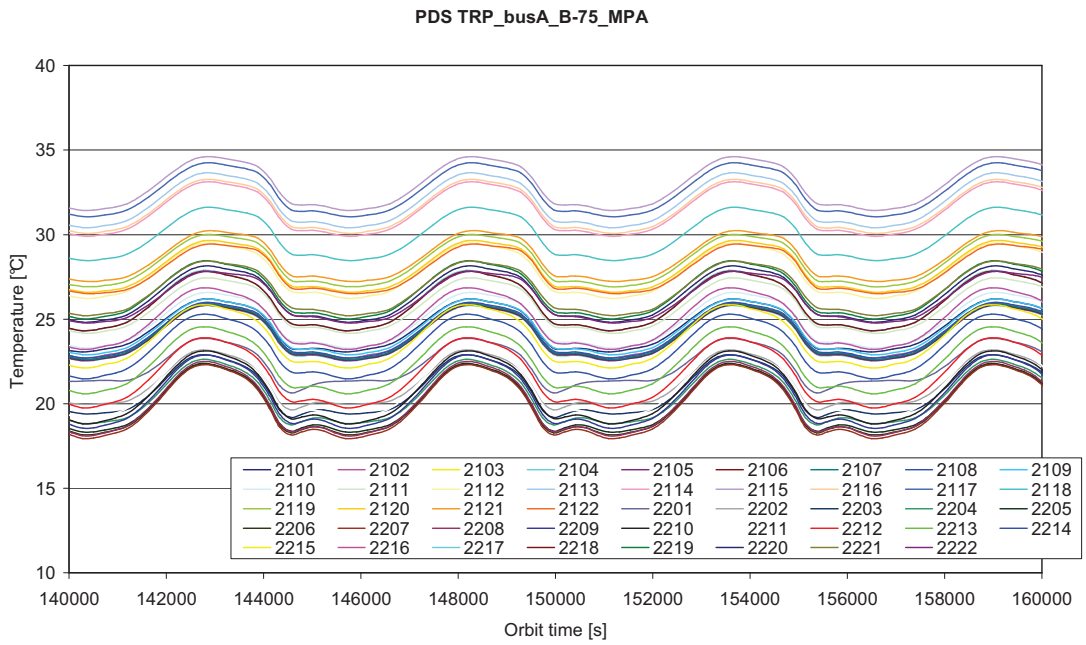

Fig 6-4 - PDS box temperature in worst hot orbit at nominal attitude - Bus B on

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	Analysis details
Analysis ID	**1**
Optical Properties	**EOL**
I/F Data Rationale	I/F data have been generated considering AMS ON in the worst HOT.
I/F Data Files	B-75_MPA_hot_wake_v.4.2
AMS Status	ON
PDS Heater power	OFF
Radiator Heater power	OFF
PDS power	365 W
CRATES power	428 W
CAB power	105 W
Results	
Max temperature PDS Bus A ON	34.2°C (2102)
Max temperature PDS Bus B ON	34.7°C (2115)

6.2 PDS POWER DISSIPATION

PDS can receive ISS power supply in a voltage range from 112V to 126V. PDS with a power supply at 112V represents the worst hot case, since the internal dissipation is higher than other cases: in this case PDS dissipates 363 W in total.

6.3 BOARDS TEMPERATURE

The following are the mean temperature of each board with the configuration above described, consider both TRP at 48°C and 53°C.

Tab 6-1 - Boards temperature results – TRP @ 53°C

PWB2_N1A	75.7 °C	PB21B	53.0 °C
PB22A	63.7 °C	PB22B	53.0 °C
PB23A	62.5 °C	PB23B	53.0 °C
PB24A	61.7 °C	PB24B	53.0 °C
ESEM3BA	55.9 °C	ESEM3BB	53.1 °C
ESEM3A1A	60.3 °C	ESEM3A1B	53.0 °C
ESEM3A2A	60.3 °C	ESEM3A2B	53.0 °C
ESEM3A3A	59.7 °C	ESEM3A3B	53.0 °C
ESEM3A4A	59.6 °C	ESEM3A4B	53.0 °C
ESEM1AA	63.9 °C	ESEM1AB	53.2 °C
CANBA	54.6 °C	CANBB	54.5 °C
INPUTSA	74.3 °C	INPUTSB	53.5 °C

Tab 6-2 - Boards temperature results – TRP @ 48°C

PWB2_N1A	70.8 °C	PB21B	48.0 °C
PB22A	58.7 °C	PB22B	48.0 °C
PB23A	57.5 °C	PB23B	48.0 °C

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PB24A	56.7 ℃	PB24B	48.0 ℃
ESEM3BA	50.9 ℃	ESEM3BB	48.1 ℃
ESEM3A1A	55.3 ℃	ESEM3A1B	48.0 ℃
ESEM3A2A	55.3 ℃	ESEM3A2B	48.0 ℃
ESEM3A3A	54.7 ℃	ESEM3A3B	48.0 ℃
ESEM3A4A	54.6 ℃	ESEM3A4B	48.0 ℃
ESEM1AA	59.0 ℃	ESEM1AB	48.2 ℃
CANBA	49.6 ℃	CANBB	49.5 ℃
INPUTSA	69.5 ℃	INPUTSB	48.5 ℃

In order to analyze the shutdown sensor (AD590) behaviour, the corresponding temperature is shown in the following table. Since no node for the sensor has been foreseen in the model, the temperature is assumed to be equal to the one of the radiator side bracket node. PB2 shutdown sensor temperature is shown in dedicated chapter.

Tab 6-3 - AD590 temperature - TRP @ 53℃

ESEM3BA	55.8 ℃	ESEM3BB	53.1 ℃
ESEM3A1A	59.8 ℃	ESEM3A1B	53.0 ℃
ESEM3A2A	59.9 ℃	ESEM3A2B	53.0 ℃
ESEM3A3A	59.3 ℃	ESEM3A3B	53.0 ℃
ESEM3A4A	59.2 ℃	ESEM3A4B	53.0 ℃
ESEM1AA	64.6 ℃	ESEM1AB	53.2 ℃
ESEM3A3A	59.3 ℃	ESEM3A3B	53.0 ℃
ESEM3A3A	59.3 ℃	ESEM3A3B	53.0 ℃

Tab 6-4 - AD590 temperature - TRP @ 48℃

ESEM3BA	50.8 ℃	ESEM3BB	48.1 ℃
ESEM3A1A	54.8 ℃	ESEM3A1B	48.0 ℃
ESEM3A2A	54.9 ℃	ESEM3A2B	48.0 ℃
ESEM3A3A	54.3 ℃	ESEM3A3B	48.0 ℃
ESEM3A4A	54.2 ℃	ESEM3A4B	48.0 ℃
ESEM1AA	59.6 ℃	ESEM1AB	48.2 ℃
ESEM3A3A	54.3 ℃	ESEM3A3B	48.0 ℃
ESEM3A3A	54.3 ℃	ESEM3A3B	48.0 ℃

Boards do not result critical from these analysis.

6.4 PB2 INTERNAL TEMPERATURE

Detailed PB2 model has been developed in order to verify that single components temperature do not exceed derated and rated temperature limits in flight and test conditions.
The following two tables show temperature limits (rated and derated) for critical element in PB2.

Tab 6-5 - PB2 internal components temperature range

Component	Derated upper limit	Rated upper limit
In Rush / Primary mosfet	110℃	150℃
Secondary / Mezzanine mosfet	110℃	150℃

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Controller	110℃	150℃
Snubber condenser	110℃	125℃
Snubber resistance	175℃	275℃
Driver transistor	110℃	150℃
Inductors	135℃	155℃ (1)
Transformer	135℃	155℃ (1)

Detailed PB2 has been analyzed using the worst power dissipation. The following tables show power dissipation distribution used for analysis and the temperature of the main nodes for both flight and test condition. As for the other board step 4.0 @ 112V has been used for power dissipation data.

Tab 6-6 - PB2 power distribution

Component	Dissipation [W]	Item quantity	Total dissipation [W]
PCB	2.00	1	2.00
INDUCTOR L3 (L OUT)	0.74	1	0.74
INDUCTOR L4 (L LEAKAGE)	6.06	1	6.06
INDUCTOR L5 (L DIFF)	0.84	1	0.84
INDUCTOR L1 (L COMMON)	0.40	1	0.40
TRANSFORMER T1	20.84	1	20.84
SNUBBER RESISTORS	6.63	1	6.63
MOSFET MEZZANIN	1.00	1	1.00
MEZZANIN PCB	1.50	1	1.50
CONTROLLER	1.00	1	1.00
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
TRANSISTOR DRIVER	0.13	1	0.13
MOSFET Q1 - Q4 PRIMARY MOS	2.53	4	10.12
IN RUSH MOS	0.52	2	1.04
MOSFET Q5 - Q8 SECONDARY MOS	2.25	4	9.00
Total power applied			**62.37 W**

Tab 6-7 - PB2 internal main node temperature

PB2 - Nodes	Test Temperature [℃]	Flight Temperature [℃]	Node Description
PWB2_N1A.T100	96.2	91.9	PCB mezzanine AUX DCDC

(1) The upper limit temperature is the lower maximum temperature of the worst material used to manufact inductor/transformer considering standard products as core, wire, capton for isolation.

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PWB2_N1A.T200	69.4	64.4	PCB mezzanine FPGA
PWB2_N1A.T300	74.8	69.9	PCB mezzanine SMALL
PWB2_N1A.T400	70.5	65.6	PCB front panel
PWB2_N1A.T811	83.6	78.6	PCB RADIATOR side
PWB2_N1A.T812	96.9	92.2	PCB RADIATOR side
PWB2_N1A.T813	76.1	71.2	PCB RADIATOR side
PWB2_N1A.T821	71.2	66.3	PCB Mid Wall side
PWB2_N1A.T822	71.0	66.0	PCB Mid Wall side
PWB2_N1A.T823	65.2	60.2	PCB Mid Wall side
PWB2_N1A.T911	83.3	78.4	Upper Bracket, Radiator Plate side
PWB2_N1A.T912 AD590 shutdown sensor	78.8	73.9	Upper Bracket, Radiator Plate side
PWB2_N1A.T1000	96.6	92.0	PCB center
PWB2_N1A.T2000	77.3	72.4	Center PCB front edge
PWB2_N1A.T3100	76.6	71.6	transformer T1
PWB2_N1A.T3101	57.1	52.1	Mosfet output Q21
PWB2_N1A.T3102	57.0	52.0	Mosfet output Q20
PWB2_N1A.T3103	56.5	51.5	Mosfet output Q25
PWB2_N1A.T3104	56.4	51.4	Mosfet output Q24
PWB2_N1A.T3110	79.0	74.1	L3 inductor
PWB2_N1A.T3120	72.4	67.5	TD2 transformer
PWB2_N1A.T3130	94.9	90.3	TD 1 transformer
PWB2_N1A.T3140	109.6	105.0	L4 inductor (L LEAKAGE)
PWB2_N1A.T3150	111.4	107.1	L5 inductor (L DIFF)
PWB2_N1A.T3160	84.5	79.8	L1 inductor (L COMMON)
PWB2_N1A.T3201	85.5	80.6	Mosfet In-rush Q10
PWB2_N1A.T3202	85.2	80.3	Mosfet In-rush Q11
PWB2_N1A.T3301	107.9	103.0	Mosfet PRIMARY Q4
PWB2_N1A.T3302	107.9	103.1	Mosfet PRIMARY Q1
PWB2_N1A.T3303	105.6	100.7	Mosfet PRIMARY Q3
PWB2_N1A.T3304	105.4	100.5	Mosfet PRIMARY Q2
PWB2_N1A.T3401	86.3	81.4	Mosfet SECONDARY Q5
PWB2_N1A.T3402	86.3	81.4	Mosfet SECONDARY Q6
PWB2_N1A.T3403	86.4	81.4	Mosfet SECONDARY Q7
PWB2_N1A.T3404	86.3	81.4	Mosfet SECONDARY Q8
PWB2_N1A.T3500	107.7	103.4	Mosfet on Mezzanine
PWB2_N1A.T3600	94.0	89.2	controller
PWB2_N1A.T3701	75.3	70.4	Tantalium Condenser
PWB2_N1A.T3702	74.6	69.7	Tantalium Condenser
PWB2_N1A.T3800	84.5	79.6	Snubber resistors
PWB2_N1A.T3901	86.0	81.2	DRIVERS transistors
PWB2_N1A.T3902	86.2	81.4	DRIVERS transistors
PWB2_N1A.T3903	86.3	81.5	DRIVERS transistors
PWB2_N1A.T3904	86.7	81.8	DRIVERS transistors
PWB2_N1A.T3905	86.9	82.0	DRIVERS transistors
PWB2_N1A.T3906	86.7	81.9	DRIVERS transistors
PWB2_N1A.T3907	85.8	81.0	DRIVERS transistors
PWB2_N1A.T3908	85.5	80.7	DRIVERS transistors
PWB2_N1A.T3909	84.8	79.9	DRIVERS transistors

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PWB2_N1A.T4000	70.9	66.0	bracket pad
PWB2_N1A.T9110	77.5	72.5	PCB board edge, Radiator side
PWB2_N1A.T9120	74.6	69.6	PCB board edge, Radiator side
PWB2_N1A.T9121	75.4	70.4	Al Plate for Transformer T1
PWB2_N1A.T9122	84.0	79.1	T bracket node
PWB2_N1A.T9130	71.6	66.6	PCB board edge, Radiator side
PWB2_N1A.T9210	56.6	51.6	PCB board edge, Mid Wall Side
PWB2_N1A.T9220	56.5	51.5	PCB board edge, Mid Wall Side
PWB2_N1A.T9230	56.0	51.0	PCB board edge, Mid Wall Side

None of the internal PB2 component exceeds derated temperature limits in flight case (TRP @ 48℃) or rated temperature range in test case (TRP @ 53℃).
In order to show the importance of the thermal interface (therm-a-form and cho-therm), the results of the analysis without these materials are proposed.

Tab 6-8 - PB2 internal main node temperature - without interface materials

PB2 - Nodes	Test Temperature [℃]	Flight Temperature [℃]	Node Description
PWB2_N1A.T100	98.9	94.6	PCB mezzanine AUX DCDC
PWB2_N1A.T200	72.1	67.1	PCB mezzanine FPGA
PWB2_N1A.T300	79.7	74.9	PCB mezzanine Small
PWB2_N1A.T400	73.1	68.2	PCB front panel
PWB2_N1A.T811	89.1	84.2	PCB RADIATOR side
PWB2_N1A.T812	104.0	99.4	PCB RADIATOR side
PWB2_N1A.T813	82.4	77.6	PCB RADIATOR side
PWB2_N1A.T821	73.9	69.0	PCB Mid Wall side
PWB2_N1A.T822	73.6	68.7	PCB Mid Wall side
PWB2_N1A.T823	68.1	63.2	PCB Mid Wall side
PWB2_N1A.T911	96.2	91.3	Upper Bracket, Radiator Plate side
PWB2_N1A.T912 AD590 shutdown sensor	92.3	87.5	Upper Bracket, Radiator Plate side
PWB2_N1A.T1000	103.0	98.5	PCB center
PWB2_N1A.T2000	81.5	76.6	Center PCB front edge
PWB2_N1A.T3100	81.6	76.7	transformer T1
PWB2_N1A.T3101	59.6	54.6	Mosfet output Q21
PWB2_N1A.T3102	59.5	54.5	Mosfet output Q20
PWB2_N1A.T3103	58.8	53.8	Mosfet output Q25
PWB2_N1A.T3104	58.7	53.7	Mosfet output Q24
PWB2_N1A.T3110	81.7	76.8	L3 inductor
PWB2_N1A.T3120	75.3	70.4	TD2 transformer
PWB2_N1A.T3130	101.4	96.9	TD 1 transformer
PWB2_N1A.T3140	116.7	112.1	L4 inductor (L LEAKAGE)
PWB2_N1A.T3150	117.4	113.1	L5 inductor (L DIFF)
PWB2_N1A.T3160	90.3	85.7	L1 inductor (L COMMON)
PWB2_N1A.T3201	98.2	93.4	Mosfet In-rush Q10
PWB2_N1A.T3202	97.8	93.0	Mosfet In-rush Q11
PWB2_N1A.T3301	121.0	116.2	Mosfet PRIMARY Q4
PWB2_N1A.T3302	121.1	116.3	Mosfet PRIMARY Q1

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PWB2_N1A.T3303	118.4	113.6	Mosfet PRIMARY Q3
PWB2_N1A.T3304	118.2	113.4	Mosfet PRIMARY Q2
PWB2_N1A.T3401	99.1	94.2	Mosfet SECONDARY Q5
PWB2_N1A.T3402	99.1	94.2	Mosfet SECONDARY Q6
PWB2_N1A.T3403	99.1	94.3	Mosfet SECONDARY Q7
PWB2_N1A.T3404	99.1	94.2	Mosfet SECONDARY Q8
PWB2_N1A.T3500	110.4	106.2	Mosfet on Mezzanine
PWB2_N1A.T3600	96.6	91.8	controller
PWB2_N1A.T3701	77.9	73.1	Tantalium Condenser
PWB2_N1A.T3702	77.3	72.4	Tantalium Condenser
PWB2_N1A.T3800	90.0	85.1	Snubber resistors
PWB2_N1A.T3901	88.7	83.9	DRIVERS transistors
PWB2_N1A.T3902	88.9	84.2	DRIVERS transistors
PWB2_N1A.T3903	89.1	84.4	DRIVERS transistors
PWB2_N1A.T3904	89.4	84.6	DRIVERS transistors
PWB2_N1A.T3905	89.7	84.9	DRIVERS transistors
PWB2_N1A.T3906	89.6	84.7	DRIVERS transistors
PWB2_N1A.T3907	88.5	83.7	DRIVERS transistors
PWB2_N1A.T3908	88.1	83.3	DRIVERS transistors
PWB2_N1A.T3909	87.5	82.7	DRIVERS transistors
PWB2_N1A.T4000	73.6	68.7	bracket pad
PWB2_N1A.T9110	86.5	81.6	PCB board edge, Radiator side
PWB2_N1A.T9120	84.7	79.9	PCB board edge, Radiator side
PWB2_N1A.T9121	80.4	75.5	Al Plate for Transformer T1
PWB2_N1A.T9122	96.8	92.0	T bracket node
PWB2_N1A.T9130	80.5	75.6	PCB board edge, Radiator side
PWB2_N1A.T9210	59.0	54.1	PCB board edge, Mid Wall Side
PWB2_N1A.T9220	59.0	54.0	PCB board edge, Mid Wall Side
PWB2_N1A.T9230	58.1	53.1	PCB board edge, Mid Wall Side

As the results show, the use of thermal interface materials are fundamental in order to obtain a significant temperature decreasing. Without thermal interface materials some temperature are above the derated limits.

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